AREA ARRAY MODULATION AND LEAD REDUCTION IN INTERFEROMETRIC MODULATORS

5   **BACKGROUND**

Interferometric modulators, such as the iMoD™, modulate light by controlling the self-interference of light that strikes the front surface of the modulator. These types of modulators typically employ a cavity having at least one movable or deflectable wall. This deflectable wall moves through planes parallel to the front wall of the cavity – the wall that is

10   first encountered by light striking the front surface of the modulator. As the movable wall, typically comprised at least partly of metal and highly reflective, moves towards the front surface of the cavity, self-interference of the light within the cavity occurs, and the varying distance between the front and movable wall affects the color of light that exits the cavity at the front surface. The front surface is typically the surface where the image seen by the

15   viewer appears, as interferometric modulators are usually direct-view devices.

Typically, interferometric modulators are constructed of membranes formed over supports, the supports defining individual mechanical elements that correspond to the picture elements (pixels) of an image. In a monochrome display, such as a display that switches between black and white, one element might correspond to one pixel. In a color display,

20   three elements may make up each pixel, one each for red, green and blue. The individual elements are controlled separately to produce the desired pixel reflectivity.

In one example of operation, a voltage is applied to the movable wall of the cavity, causing it be to electrostatically attracted to the front surface which in turn affects the color of the pixel seen by the viewer. A difficulty exists in producing modulators with accurate and

25   repeatable mechanical properties, so that specific applied analog voltages produce specific analog displacements of the movable wall that acts as a mirror at the back of the interferometric cavity. To produce accurate and repeatable color combinations, typical

modulators use only binary displacement of the movable mirror. In this mode of operation any given movable mirror-wall will be found at rest in either its quiescent state where it produces one of the color states mentioned above or its fully deflected state where it produces a black optical state.

5   Thus these binary operated modulators are capable of displaying only two gray levels per pixel, such as black and white in the case of a monochrome modulator, or eight colors per pixel, such as red, green, blue, cyan, yellow, magenta, black, and white for example, in the case of a color modulator. It is desirable to display additional shades of gray in a monochrome display and additional colors in the case of a color display. Since controlling

10   analog deflection of the single monochrome mirror per pixel or three-color mirrors per pixel can be unreasonably difficult it becomes necessary to devise a modulator architecture with a more complex pixel structure.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention may be best understood by reading the disclosure with

15   reference to the drawings, wherein:

Figure 1 shows an example of an interferometric modulator.

Figure 2 shows a prior art implementation of an area-ruled LCD modulator pixel, including its corresponding connection leads.

Figure 3 shows an embodiment of an interferometric modulator using area array

20   modulation having reduced leads.

Figure 4 shows a timing diagram for a multiplexed interferometric modulator.

Figure 5 shows another embodiment of an interferometric modulator using area array modulation having reduced leads.

Figure 6 shows a timing diagram for an interferometric modulator using equally

25   weighted regions.

Figure 7 shows another embodiment of an interferometric modulator using area array modulation.

Figures 8a-8c show an embodiment of electrically cascaded interferometric modulator elements.

5   Figure 9 shows an embodiment of deflectable elements similar to interferometric modulator elements used as switches.

Figure 10 shows a graph illustrating how deflectable elements can be selectively addressed by varying amplitude and duration of voltage pulses.

DETAILED DESCRIPTION OF THE EMBODIMENTS

10   Figure 1 shows an example of an interferometric light modulator. This particular example is an iMoD™, but any interferometric modulator may utilize the embodiments of the invention. No limitation or restriction to iMoD™ modulators is implied or intended.

The modulator is typically comprised of an array of individual elements arranged in rows and column. One element shown in Figure 1 has an electrode layer 12 on a transparent

15 substrate 10, typically glass. One surface 14 of the modulator's optically resonant, interferometric cavity is fabricated on the electrode layer and an oxide layer 16 covers this surface. The parallel surface of the cavity, mirror 20, is suspended above the cavity by supports 18. In operation, when the electrode on the glass substrate is activated, the mirror 20 is electrostatically attracted toward the glass substrate. The deflection of the mirror 20

20 changes the dimensions of the cavity and causes the light within the cavity to be modulated by interference.

The resulting picture element (pixel) from a direct-view display will be composed of elements such as the one shown in Figure 1. Each of these modulator elements with the mirror 20 in an undeflected state will be bright, or 'ON.' When the mirror 20 moves to its

25 full design depth into the cavity toward the front surface of the cavity, the change in the cavity causes the resulting pixel to be 'dark' or OFF. For color pixels, the ON state of the

individual modulating elements may be white, red, green, blue, or other colors depending upon the modulator configuration and the display color scheme. Most typically a single color pixel will be composed of a number of modulator elements that create interferometric blue light, a similar number of elements that create interferometric red light, and a similar number

5   that create interferometric green light. By moving the mirrors according to display information, the modulator can produce full color images.

The most basic display activates simultaneously all modulator elements of a given color within a pixel with the result being that eight colors per pixel are possible. The current invention provides for the activation within a pixel of some elements of a given color

10   separately from other elements of that same color. This enables multiple intensities of red light, multiple intensities of blue light, and multiple intensities of green light to be mixed within a given pixel. The result is that rather than being limited to 8 colors per pixel the interferometric display is capable of thousands of colors per pixel.

Similar types of area-weighted modulation have been practiced in other types of

15   displays. For example Figure 2, which corresponds to Figure 9 in US Patent No. 5,499,037, shows an area-weighted method. In this example, 16 levels of intensity are provided by creating a subpixel containing 9 separate pixel elements addressed with six electrodes, three formed as horizontal connecting leads and three formed as vertical connecting leads. A full-color pixel formed this way might have 9 vertical leads, three for red, three for green, and

20   three for blue, and the same three horizontal leads shown in Figure 2. This pixel provides 4096 colors (16x16x16), but with 12 leads it would result in a much more complex display system than would a pixel with four leads providing eight colors.

Because the individual elements of interferometric modulators tend to operate in a binary mode, bright in a quiescent state and dark in a fully deflected state, analog operation is

25   not readily available. Therefore, interferometric modulators are likely to benefit from an area-ruled method of operation. It is one purpose of embodiments of this invention to provide

a method of area-ruled operation that is uniquely suited for application to interferometric modulators and which reduces the complexity required by previous implementations.

One embodiment of an interferometric modulator area-ruled architecture requiring fewer pin outs and still providing higher bit depth is shown in Figure 3. Driver device 50 has one output pin per display row, and a connection line is provided between each driver device output pin and a corresponding row of the modulator array. The single row connection is multiplexed between the sub-elements that comprise the sub-rows of the display element. The term display element has been introduced here to specify a certain area of the entire display surface. The display element is a collection of sub-elements, that typically resolves into a portion of the display presenting a coherent set of image information. The most typical display element would correspond to a single pixel in the resulting image. The display element 40 in Figure 3 has been divided up into three columns, 42, 44, and 46, typically one for each color such as red, green and blue, in the case where 40 represents a pixel. In addition, each column has been divided up into 4 sub-elements arranged in sub-rows.

To understand how the system in Figure 3 functions, consider that the row select outputs of driver device 50 typically become active in a sequential pattern starting with output 1, then proceeding to output 2 and so on. When the timing signals cause row 5 to become active, the switch 56 closes and switch 58 becomes open, causing the active driver pin voltage to be applied to the sub-row of sub-elements 42a, 44a and 46a. Simultaneously, the data lines 43, 45, and 47, which may be connected to a driver device not shown in Figure 3, are driven with the proper voltages to cause the sub-elements 42a, 44a, and 46a to switch to states appropriate to the current image content associated with display element 40.

As soon as sub-elements 42a, 42b, and 42c have reached their newly addressed positions switch 56 opens and switch 58 closes. Immediately thereafter switch57 closes and switch 59 opens, and the data lines 43, 45, and 47 are driven to the appropriate values for sub-pixels 42b, 44b, and 46b. This sequence continues until the three data lines have been driven

with the four different data sets to update the twelve sub-pixels in display element 40. Then

this sequence repeats for rows 6, 7, and so on.

As shown in Figure 3 the timing/switch-activation signals are shared with all other

rows throughout the display, so that switches for the first sub-row of every row toggle when

5 the first sub-row of any row is active, and so on for the second, third, and fourth sub-rows.

However, only the driver output pin for the active row is energized with the active addressing

voltage level. All non-active rows are held to a non-select bias voltage while the active row

is elevated to a data select voltage. In this manner, elements in all sub-rows except the

active sub-row see the same, non-select voltage independent of the status of the timing

10 signals and consequently independent of the positions of the switches within the sub-row. It

should be observed that switching of the non-active, row-select switches could be avoided

with masking circuits in cases where ultimate low power consumption is desired

As can be seen from Figure 3, the switches 56 and 58 as well as the other switches

connected to the timing signal lines, are manufactured to be microelectromechanical devices

15 similar to the interferometric elements, such as the one shown in Figure 1. Because the array

is undergoing microelectromechanical processing to create the interferometric display

elements, manufacturing these 'extra' elements in the area surrounding the array would not

create extra complexity or necessarily raise the cost of the device. It is possible that the

multiplexing of the sub-rows could be done with other types of switches, including but not

20 limited to microelectromechanical switches fabricated in a manner not similar to the

fabrication of the interferometric elements and more conventional electronic switches

fabricated using thin silicon films deposited on the modulator's glass substrate.

The term 'similar to' as used here means that the devices have the same basic

structure of an electrode, a cavity, and a mirror suspended over the cavity. When

25 constructing an electrical switch, the optical functionality fabricated near the glass substrate

in an interferometric modulating element is not required, and it may be desirable to eliminate

this optical functionality. It is only required that at full deflection the mirror come in contact with (and hence connect electrically) two conductive areas, most likely fabricated from the thin film layers used to fabricate the addressing electrodes and/or a conductive layer used to form the front wall of the optically resonant cavity. This is different than the way the

5   interferometric element may operate, which is why the switch structure is 'similar to' rather than the same as the display element.

A timing diagram for one possible operation of row 5 is shown in Figure 4. At t_0, the signals for row 4 are high, as seen from the modulator. At t_1, the signal for row 4 goes low and row 5 becomes active. Similarly, the line for row 5A becomes active. At t_2, row 5A goes

10   low and row 5B becomes active. This continues in series for rows 5C and 5D.

This embodiment results in a reduced number of connections between the array and the driver. The connections necessary to drive the individual sub-elements in the sub-rows are made in the surrounding area of the modulator array, bringing them 'on-chip' with the array, rather than requiring the driver device to provide separate output pins for each sub-

15   element.

The sub-elements shown in Figure 3 have been drawn to be of approximately equal areas. Another useful geometry uses sub-elements with binary 'physical' weighting relative to each other. As can be seen in the display element 70 of Figure 7, a bit depth of 4 is provided using only 4 such sub-elements. For example, area 78 has a size approximately

20   equal to one-half the full size of display element 70. Sub-element 74 has a size approximately equal to one-half the size of the next largest sub-element, in this case, sub-element 78, giving sub-element 74 a size one-quarter of the full-size display element. Each subsequent sub-element has a size approximately equal to one-half the size of the next largest sub-element. Sub-element 72 is one-half that of 74, or one-eight that of 70. Sub-element 71

25   is one half of 72, or one-sixteenth of 70.

The elements having different physical sizes are activated as needed to achieve an overall display pixel with a given color intensity. The table below shows the ON sub-elements, by reference number for each color intensity level.

Color intensity	Sub-elements ON
0	None
1	71
2	72
3	71, 72
4	74
5	71, 74
6	72, 74
7	71, 72, 74
8	78
9	71, 78
10	72, 78
11	71, 72, 78
12	74, 78
13	71, 74, 78
14	72, 74, 78
15	71, 72, 74, 78

5   Although described here as being addressed by the multiplexing technique of Figure 3 this implementation of area weighting can be used separately from the multiplexing technique described above. Increased interconnection complexity will result, but this relatively low level of complexity will be acceptable in many systems.

In an alternative embodiment, the bit depth of 4 is achieved by dividing each sub-

10   column for a display element into 16 (2^4) sub-elements. Each set of 16 sub-elements in each sub-column are connected together in a cascading fashion and are therefore referred to as 'sub-element cascades.' The individual cascaded sub-elements may be fabricated to serve as both interferometric modulating elements and electrical switches such as those shown in Figure 3. Alternatively, each individual interferometric sub-element may have an electrical

15   switch fabricated immediately adjacent.

An example of a display element 60 having sub-element cascades for 4 bits of depth is shown in Figure 5. The three column lines connect to the first element in a sub-element

cascade; sub-element 61r is the first element in the red cascade, 61g in the green cascade and 61b in the blue cascade, the last elements being 615r and 616r for the red cascade. The control of color intensity is provided by the width of an addressing pulse applied to the column line. This may be best understood by looking at two possible sub-element

5   configurations shown in Figure 8 and Figure 9.

In Figure 8a sub-element members of a sub-column, such as the sub-elements 61r, 62r, and 63r shown in Figure 5, are shown in cross-section. The interferometric cavity is defined by the suspended, movable mirror elements such as 82 and the front surface optical film stacks such as 84. In this case the suspended movable element also functions as the

10   contactor of a switch as did the switches shown in Figure 3. Arrayed within each sub-element, adjacent to the optical film stack, are conductive elements 86a-86e. When the movable mirror 82 comes in contact with the optical film stack 84 the sub-element has switched from one optical state to a second optical state. Additionally, a circuit is completed, since the movable mirror now connects conductor 86a to conductor 86b.

15   The sub-element cascade is addressed by applying one polarity of an address voltage to the moving mirror 84 and the fixed contact 86a. The second polarity of the address voltage is applied to an electrode within or below the optical film stack 84. The resultant potential difference causes mirror 82 to deflect, completing the connection between conductor 86a and 86b as shown in Figure 8b. With the first voltage polarity now applied to conductor 86b

20   (through mirror 82), mirror 92 will eventually deflect as shown in Figure 8c. This process will continue until all of the cascaded mirrors have collapsed or until the address pulse is removed. Thus the reflective intensity of the display element is controlled by controlling the time duration (or pulse width) of the address pulse.

Figure 6 shows a timing diagram for three successive addressing sequences of a sub-

25   element cascade with color values of 12, 13, and 3 respectively. A color value of 0 is 'black' or OFF, and a color value of 16 would represent all sub-elements of the cascade being on.

The addressing pulse is shown in the top line. As can be seen, as the time duration of the address pulse increases more mirror elements are activated, moving into the 'black' or OFF state. During the first address pulse, four elements move into the 'black' state, and a color value of 12 is achieved – 12 elements are left in the bright state. Taken in light of Figure 5

5 this might correspond to sub-elements 61r, 62r, 63r, and 64r switching successively to the 'black' state.

During the second addressing, the address pulse is shorter, and only three elements switch to the 'black' state. In the final addressing, 13 elements switch to the 'black' state leaving a fairly dark reflectance color value of three. The discontinuity in the timing diagram

10 represents the relatively long period (typically a 'frame time' in video terms) that the mirrors remain in their addressed states. It is during this integration time that the viewer's eye becomes impressed with the area weighted intensity value.

At the end of each frame time, Figure 6 shows that all of the mirrors are reset to their quiescent position before being addressed again. It is possible to address the interferometric

15 device so that this reset is not necessary. It is included here to emphasize the switching operations that take place during each 'line time' of addressing. It should be noted that the address pulse must exceed a certain minimum time duration in order to cause the first element in a sub-element cascade to turn ON. A very short addressing pulse, such as a transient signal, that is shorter than the response time of the sub-elements, will not cause the first sub-

20 element to switch.

Once the address pulse has been active long enough for the first sub-element to switch, the addressing signal is 'passed on' to the next element in the array. Again, the address pulse must be active long enough past the switching of the first element to cause the second element to switch. As the response times of the sub-elements are assumed to be

25 approximately the same, the sub-element cascade should be controllable to provide a desired number of sub-elements to turn ON while providing a relatively high immunity to spurious

signals. The cumulative effect is to cause the display element to form the proper color intensity in the resultant pixel. In this manner, a display element with a bit density of 4 was made possible without any extra connection lines or extra connections from the driver device.

The cascade effect described above is based upon movable mirror elements that

5   provide both the optical function of the display as well as the electrical switching cascade itself. An alternative, shown in Figure 9, is to provide adjacent to each interferometric sub-element such as 100 a separate electrical switch such as 102 that toggles simultaneously with the optical element. The embodiment of Figure 9 shows a micromechanical switch, but other types of switches, such as silicon or other semiconductor transistor switches may be used as

10   well. In this way the parameters of the optical element and the parameters of the electrical element can be separately optimized. The addressing waveforms and color value results of the system of Figure 9 are identical to those provided by the system of Figure 8. The systems of Figures 8 and 9 are both examples of obtaining different levels of bit-depth by controlling the behavior of the modulator over time.

15   In Figure 10 a graph is provided to illustrate that by varying the time duration of addressing pulses as well as the voltage levels of those pulses a more refined control of movable mirror addressing for bit-depth switching can be implemented. Figure 10 applies to a display element consisting of several individual moving mirrors. The mirrors are denoted by the names b_1, b_2, b_3, etc. The mechanical support structure of the mirrors as well as the

20   mirror element themselves can be manufactured using a number of different techniques, such as varying film thickness and residual stress within the film, to allow individual mirrors to deflect at different rates versus time and at different displacements versus applied voltage.

As shown in Figure 10 movable element b_1 deflects after a short application of voltage V_1. Mirror b_2 responds more slowly and will activate after a longer application of V_1. Both

25   mirrors b1 and b3 will respond to a brief application of V_2, and mirror b_4 is capable of responding to a very quick application of V_2 to which none of the other mirrors can respond.

In this way various combinations of mirrors can be deflected by shaping address pulses in the time/voltage space, where the term 'combination' includes the switching of a single element. If these mirrors have different areas, such as the areas shown in Figure 7, then multiple brightness levels can be achieved by addressing a multi-segment display element with a single pair of electrical connections.

In all of these manners, alternative methods of providing intensity bit depths far beyond a single bit can be accomplished for interferometric elements. While the implementations above were discussed with regard to a bit-depth of 4, having 16 levels of color intensity, these embodiments may be employed for any bit-depth greater than 1.

Thus, although there has been described to this point particular embodiments for a method and apparatus for area array modulation and reduced lead count in interferometric modulators, it is not intended that such specific references be considered as limitations upon the scope of this invention except in-so-far as set forth in the following claims.